IDEC Chip Design Contest

12-bit 10-MS/s CMOS Pipelined ADC

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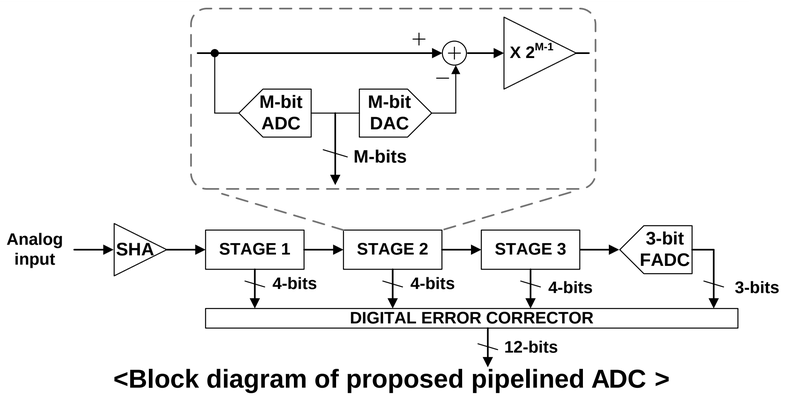
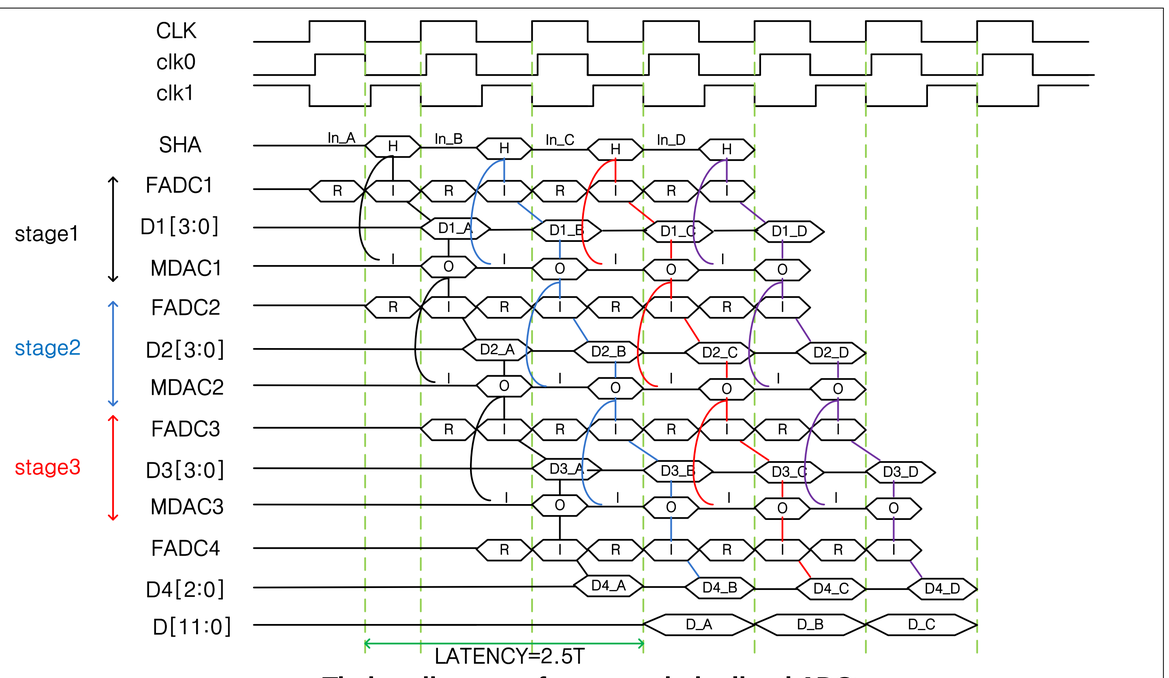
Block and Time Diagrams of Proposed Pipelined ADC

Block and Timing Diagrams Proposed Pipelined ADC



<Block diagram of proposed pipelined ADC >

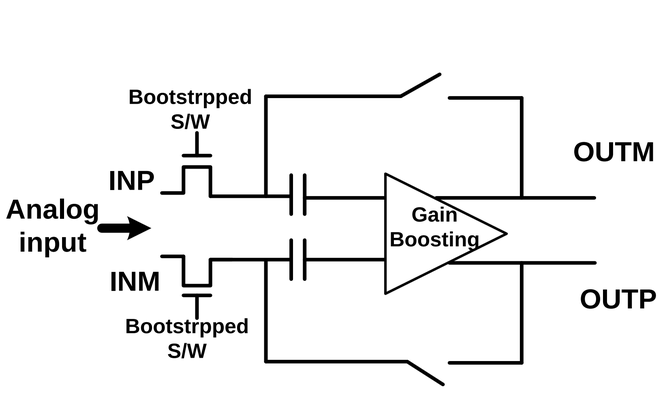
- Proposed pipelined ADC consists of 3-stage structures that produce binary code of 4-bits(stage 1-3) and 3-bits flash ADC.
- All stages consist of multiplying DAC(MDAC) and flash ADC(FADC).
- Digital error corrector calculates and generates from the binary code of each stage to the binary code of 12 bits.
- The latency of 2.5T is required until the 12-bit data is converted and output.



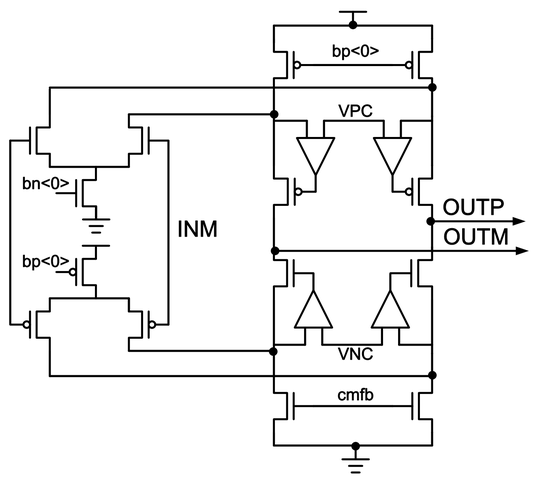
<Timing diagram of proposed pipelined ADC>

Building Block

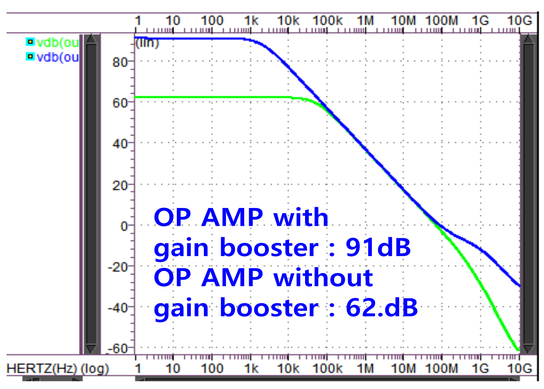
Sample and hold amplifier with gain boosting



<Block diagram of SHA>



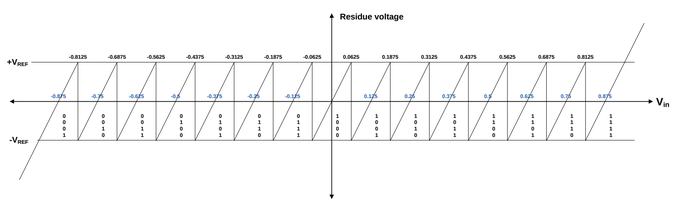
<Circuit diagram of gain boosting amplifier >



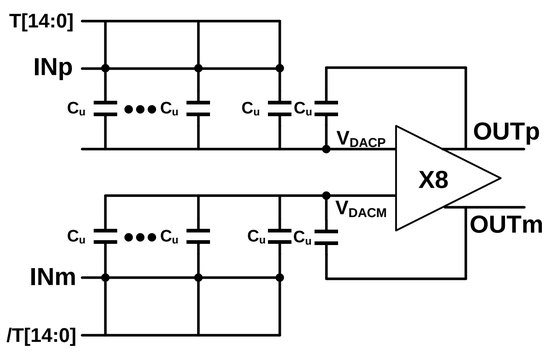
<Simulation result of gain boosting amplifier >

- Gain boosting amplifier
  - Output resistance is increased by using feedback OP amplifier in the output stage.
  - The increased output resistance boosts the low frequency voltage gain of the OP amplifier from 62.1dB to 91dB.
  - Gain boosting amplifier reduces the gain error of the sample and hold amplifier for the 12-bit pipelined ADC.

Multiplying DAC block diagram



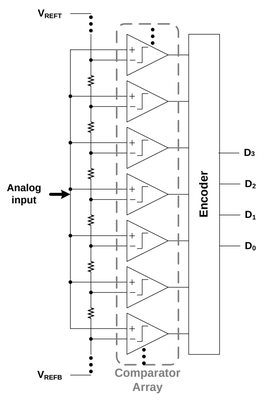
<Residue voltage of multiplying DAC >



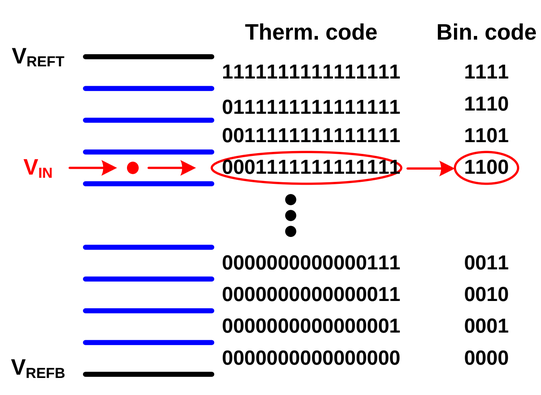
<Timing Diagram>

- Thermometer code from FADC passed through the CDAC and changes to the residue.
- The generated residue is amplifier to match the input swing voltage.
- Stage that generated the binary code of n-bits should amplify 2^{n-1} times.

Flash ADC



<Block diagram of Flash ADC>

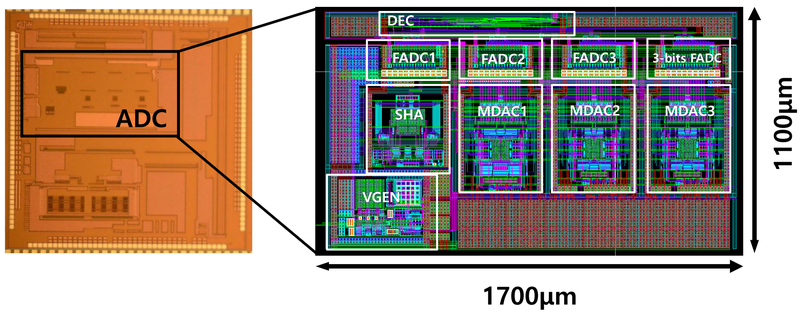


<Operation of Flash ADC>

- Flash ADC creates the thermometer code.
- Encoder converts the thermometer code to the binary code.

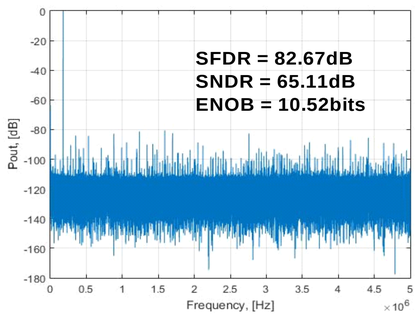
Chip Implementation and Measurement Results

Chip Implementation

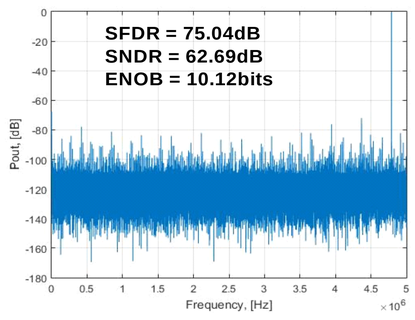


- Process & Supply: 180-nm 1-poly 5-metal CMOS process w/ MIM capacitor and 1.8V supply voltage
- Power consumption: 20mW
- Core area: 1700 ㎛ × 1100 ㎛

Measurement Results



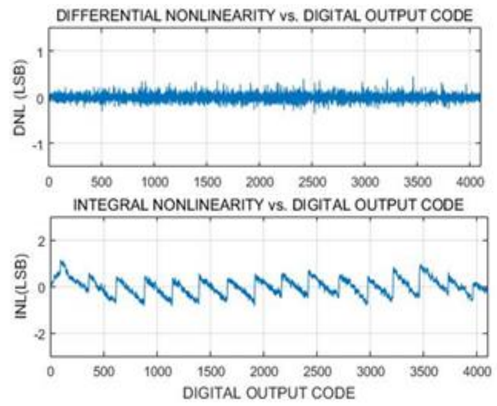
(a)



(b)

<Output spectrum for input signal with (a) low frequency (b) Nyquist frequency>

- Low input frequency
  - SNDR = 65.11dB
  - ENOB = 10.53bits
- Nyquist input frequency
  - SNDR = 62.69dB
  - ENOB = 10.12bits



<Measured (a) DNL and (b) INL>

- DNL = -0.35/0.45 LSB
- INL = -0.84/1.16 LSB

※ This research was conducted using the MPW program and CAD tools supported by IC Design Education Center (IDEC).

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